REMARKS/ARGUMENTS

Interview: The Applicants thank the Examiner for his courtesy and consideration in discussing this Application in informal telephone interview on January 13, 2006. The claims, as amended, were discussed. The focus of the discussion was whether the cited references teach the machine code instruction of the present claims. While no agreement was reached, the Applicants thank the Examiner for the opportunity to discuss the issues. Further, the Applicants respectfully request that the Examiner refer to the discussion below, as a closer examination of the reference revealed additional clear evidence that the limitations of the claims are not disclosed in the reference

Status of the Claims

Before this Amendment, claims 1-21 were present for examination. Claims 1, 8, and 18 are amended. No claims are canceled, and no new claims are added. Therefore, claims 1-21 are present for examination, and claims 1, 8, and 18 are the independent claims. No new matter is added by these amendments.

The Office Action rejected claims 1-21 under 35 U.S.C. §102(a) as being anticipated by the cited portions of U.S. Patent No. 6,889,242 to Sijstermans et al. ("Sijstermans"). The Office Action also rejected claims 1-21 under 35 U.S.C. §112, second paragraph. The Applicants respectfully request reconsideration of this application as amended.

35 U.S.C. §102(a) Rejection, Sijstermans

The Office Action rejected claims 1-21 as being anticipated by Sijstermans. The claims have been amended to recite certain embodiments of the invention more particularly. Support for the amendment is found in the Specification (Original Application, p. 8, ll. 7-33; Fig. 4. For a valid anticipation rejection, the Office must show that each limitation from the claims appears in a single piece of prior art. The Applicants believe limitations from the amended independent claims are neither taught nor suggested in the reference.

Specifically, claim 1 is amended to recite a single, executable "machine code instruction comprising an address for the first input register, an address for the second input register, an address for the output register, the op code indicating a function to perform, and the rounding factor." Claims 8 and 18 contain similar limitations. With these modifications, it is clear that the limitations of the amended claims are *not* disclosed in the cited art.

Sijstermans describes a VLIW processor able to execute a rounded averaging operation of four unsigned byte vectors (Sijstermans, col. 6, ll. 9-14). However, in Sijstermans, a "single **machine instruction** can be used to **select** one of a variety of rounding modes. ... Once a rounding mode is set, the programmable processor uses the mode when executing **subsequent machine instructions that perform arithmetic operations**" (emphasis added)(*Id.*, col. 2, ll. 33-45). Sijstermans clearly suggests a ***first*** machine instruction to select a rounding mode, and ***other*** instructions to perform the arithmetic operation. Claims 1, 8, and 18 instead specify a **single executable machine code instruction** including a rounding factor and the op code and addresses for the operation.

Moreover, the Office identified "avg4_bu rsrc1 rsrc2 rsrc3 rsrc4" and "avg4_bu r10 r20 r30 r40" as reading on the single machine code instruction limitation. But there is no rounding factor contained in either of these instructions, as they merely appear to be executing an operation with a *previously selected* rounding mode. Moreover, these instructions merely represent "syntax." Each instruction appears to merely be some sort of assembly language syntax, and there is no teaching or suggestion that this syntax necessarily corresponds with a single machine code instruction.

35 U.S.C. §112, Second Paragraph Rejection.

The Office Action rejected claims 1-21 under 35 U.S.C. §112, second paragraph. The claims were amended to address this rejection

CONCLUSION

The present invention presents a "novel computer processor chip having a sub-instruction for performing pixel average functions in parallel. As one skilled in the art will

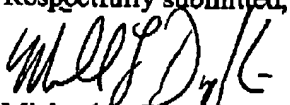
appreciate, performing multiple pixel average functions in a single instruction issue increases efficiency" (Original Application, p. 3, ll. 1-4). The claims recite a novel machine code instruction configuration that is clearly not suggested by the reference.

Therefore, the Applicants respectfully submit that the specified limitations in independent claims 1, 8, and 18 are not taught or suggested in Sijstermans. These claims are allowable for at least these reasons. Claims 2-7, 9-17, and 19-21 each depend from these independent claims, and are believed allowable for at least the same reasons as given above.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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